DSP-based PLL-controlled 50–100 kHz 20 kW high-frequency induction heating system for surface hardening and welding applications

N.S. Bayındır, O. Kükrer and M. Yakup

Abstract: A digital signal processor (DSP)-based phase-locked loop (PLL)-controlled high-frequency induction heating system is described. The rectifier and insulated gate bipolar transistor (IGBT) inverter are controlled by a TMS320F240 DSP system, which has the hardware feature of providing a dead-band delay independent of the frequency of operation. This feature, together with the high speed of the DSP, allows the use of zero current resonant switching at a high power factor for frequencies up to 100 kHz. Resonant operation of the inverter is maintained by a simple digital PLL scheme implemented on the DSP. The frequency converter enables safe operation at all load conditions with digital overcurrent, overvoltage and overtemperature protection features. The cost-effective system described is operated successfully at outputs up to 19.8 kW at 72 kHz and 500 V.

1 Introduction

High-frequency induction heating furnaces are widely used in applications such as surface hardening, welding, metal to plastic or metal to glass bonding and curing. The higher efficiency, very short heating times and local heating capabilities of induction heaters have made them superior to other heating devices. With the latest advances in power semiconductor switching devices and microprocessors, high-frequency induction heating power supplies are now more reliable and cost-effective and have higher performances [1–4]. In [4] a pulse amplitude modulated voltage source, series load resonant inverter has been developed using high-power static induction transistors (SITs), which operates at a load-adaptive tuned operating frequency that is slightly higher than the series resonant frequency in order to achieve zero-voltage soft-switching commutation. A phase-locked loop integrated circuit (PLL-IC) is used to provide load resonant operation based on the phase-locked loop principle. Due to the difference between the switching frequency and the load resonant frequency, the power factor has been degraded by 5% and oscillations are observed at the switching instants. Moreover with this method the delay between the inverter output voltage and current waveforms cannot be maintained at the same level at all frequencies due to the change in component characteristics with frequency. In [1], a half-bridge inverter circuit with series–parallel resonance is described which does not use an impedance matching transformer. Series and parallel compensating capacitors are used to reduce the reactive loading of the workpiece and also to increase the load current with respect to the inverter current. However, the method is valid for coil inductance values less than twice the total series stray inductance in the circuit. Another disadvantage is the use of an extra capacitor, which is expensive at the frequencies in question. A comparison of series and parallel inverter systems [5] has revealed that the voltage source series resonant inverter offers better overall performance than the parallel resonant counterpart with respect to converter utilisation. Considering the results of this comparison, the series resonant inverter topology has been adopted in this project.

In this paper digital signal processor (DSP)-based PLL control scheme is presented in which the phase difference between the inverter voltage and current is minimised and made independent of the operating frequency. The hardware dead-band feature of the DSP is used, in conjunction with software-based PLL control, to achieve precise zero-current switching operation so that the $\frac{di}{dt}$ stresses on the insulated gate bipolar transistors (IGBTs) are minimised and switching occurs with negligible oscillations. The DSP-based digital control approach enables easy implementation of various monitoring and protection functions, in addition to the built-in dead-band feature. Furthermore, a digital implementation of the PLL scheme is more reliable than an analogue implementation, where changing component characteristics may degrade performance in time. Moreover, in analogue implementations of PLL control the dead-band time may vary with operating frequency, which then degrades the power factor.

The design and constructional features of the whole system are presented in this paper. Experimental work has been carried out on the induction heating system to measure the operational performance under various loading conditions. Experimental results indicate that the system operates successfully with a power factor very close to unity. A simulation model has been developed using Simulink, which has been used to analyse and design the PLL control system. A mathematical model of the system has also been developed in discrete time, with which the stability of the system can be assessed.
2 System description

The general layout of the frequency converter is shown in Fig. 1, where it may be seen that the output power is controlled by a three-phase controlled rectifier and that the inverter is of the voltage-fed load resonant type. High-speed IGBTs with fast anti-parallel diodes are used in the inverter. RC snubbers are used to reduce the $dv/dt$ stresses on the IGBTs. A high-frequency impedance matching transformer with a turns ratio of 5/1 has been designed and constructed with an amorphous core on which the primary and secondary coils are wound using Litz wire, and this is used to isolate and match the impedances of the converter and the induction heating coil. The induction heating coil and the impedance matching transformer are water cooled. A high-frequency compensating capacitor of value $C_s = 1 \mu F \ (500 \text{kHz}, 600 \text{V})$ is connected in series with the coil ($L_s$). The inverter output voltage and the capacitor voltage are measured by means of high-frequency voltage transducers to provide the necessary inputs to the DSP for PLL control. The inverter and coil currents are also measured to track the load resonant operation and also to measure the efficiency of the converter and of the impedance matching transformer.

3 DSP-based PLL control system

3.1 Control system description

A simple DSP-based PLL control algorithm has been developed in which the dead-band delay is provided by the special hardware feature of the TMS320F240 DSP system. The digital implementation of PLL maintains resonant operation over a wide range of frequencies from 50 to 100 kHz. A block diagram of the PLL system is shown in Fig. 2. The capacitor voltage $v_c$ and the inverter output voltage $v_i$ are measured with high-frequency voltage transducers with negligible delay and the zero crossings of these voltages are detected and compared in an XOR gate, as shown in Fig. 3. The output of the XOR gate is filtered to yield a DC voltage $x_f$ proportional to the phase difference between the inverter and capacitor voltages. This voltage is isolated optically and applied to the analogue input of the DSP, where digital implementation of the PLL scheme is then realised. The flowchart of the PLL control algorithm is shown in Fig. 4. The voltage input to the DSP, which is proportional to the phase difference between the inverter output and the capacitor voltages, is compared with a value corresponding to 90 degrees and the switching frequency is adjusted so that this difference is made zero. When this condition is achieved, the capacitor and the inverter voltages are in quadrature, which ensures that the inverter voltage and current are in phase.

The pulse width modulated (PWM) outputs of the DSP are used to generate switching pulses for the inverter IGBTs. The PWM periods determined by the PLL algorithm are loaded into the timer control register T1CON, which then starts generation of the PWM
switching pulses. The dead-band delay between the switching instants of the IGBTs on the same leg of the inverter is provided by the dead-band control register DBTCON, which is set at 0.8 μs. This delay is adjusted by the special hardware feature of the DSP, and is independent of the processing delays. This feature of the DSP maintains a constant delay at all frequencies, which is not possible in analogue circuit implementations of PLL control due to the variation of component characteristics with frequency (particularly in the high-frequency range). The DSP operates at a speed of 20 MIPS, which makes it possible to control the system up to 100 kHz.

During experimentation, a lower frequency limit of 50 kHz and an upper frequency limit of 100 kHz were set on the control system so that the operating frequency could never exceed these limits accidentally. The switching signals are isolated and amplified before they are applied to the gates of the IGBTs using a signal conditioning circuit.

3.2 Mathematical model

An approximate discrete-time model of the system was found to be useful in designing the control system. Referring to Fig. 4, the PLL control is implemented in discrete-time by the following equation:

\[ T(k + 1) = T(k) + K_e e(k + 1) \]  

which corresponds to integral action.

In (1) \( T \) is the inverter voltage period (represented by \( T_i \) in digital form in Fig. 4), \( K_e \) is the integral gain (represented by \( K_{eD} \)) and \( e \) is the error in phase difference (represented by \( e_{\phi D} \)) defined as:

\[ e(k) = x_f(k) - \frac{1}{2} \]  

where \( x_f \) is the average value of the normalised LP filter output (Fig. 5).

![Fig. 5 Waveforms for PLL operation](image)

Normalisation here refers to a scaling such that the maximum is unity (corresponding to 100% duty ratio of the XOR output). Note that the period of the VCO output (\( T \)) is updated instead of its frequency. This is found to be more convenient since the inverter control program (dead band) requires period information directly.

Now, it is clear that \( x_f \) can be expressed in the steady state in terms of the phase difference \( \phi \) as

\[ x_f,ss = \frac{\phi}{\pi} = u_f \]  

where \( u_f \) is the average value of the LP filter input.

\[ \frac{df_x}{dt} = \frac{1}{\tau_f} x_f + \frac{1}{\tau_f} u_f \]  

where \( \tau_f = R_f C_f \) is the time constant of the filter.

Note that in (4) \( u_f \) is a function of the frequency of the inverter voltage (or its period) through the phase difference \( \phi \). Considering the steady state operation of the resonant load of the inverter, the following relationship can be obtained between \( \phi \) and \( T \):

\[ \phi(T) = \tan^{-1}\left( \frac{2\pi R_f C_i}{1 - \left(\frac{2\pi f}{\omega_0}\right)^2} \right) \]  

where \( \omega_0 = 1/\sqrt{L_i C_i} \); \( L_i \) is the inductance of the heating coil and \( R_i \) is its equivalent resistance.

It is assumed that the relationship (5) is approximated valid during transient operation in which the period \( T \) changes slowly. Furthermore, (5) is obtained by assuming that the inverter output voltage is purely sinusoidal.

Equation (4) can be discretised as follows:

\[ x_f(k + 1) = a x_f(k) + b \frac{\phi(T[k])}{\pi} \]  

where \( a = e^{-T_s/\tau_f} \), \( b = (1-a) \), and \( T_s \) is the control sampling time. Using (1), (2) and (6) the closed-loop system equation is obtained as

\[ T(k + 1) = T(k) + K_e \left[ a x_f(k) + b \frac{\phi(T[k])}{\pi} - \frac{1}{2} \right] \]  

Equations (6) and (7) are non-linear, since \( \phi \) is a non-linear function of \( T \). These equations can be linearised easily by linearising (5) around the operating point, where the inverter frequency is equal to the resonant frequency of the load, to give (see Appendix, Section 7)

\[ \phi(T) \approx \frac{\pi}{2} - \frac{1}{\pi R_i C_i} (T - T_0) \]  

where \( T_0 \) is the inverter period at the operating point.

With the following definitions of perturbation variables:

\[ \Delta x_f = x_f - \frac{1}{2} \]  

\[ \Delta T = T - T_0 \]  

the linearised closed-loop equations of the system become (see Appendix, Section 7)

\[ y(k + 1) = A_x y(k) \]  

In (10) \( y \) is the column vector \( y = [\Delta x_f \ AT]^T \) and

\[ A_x = \begin{bmatrix} a & -\frac{1-a}{\pi^2} \tau_f \frac{1}{2} \\ a K_e & 1 - \left(\frac{2\pi f}{\omega_0}\right)^2 \end{bmatrix} \]  

where \( \tau_f = R_f C_f \).

Applying Jury’s stability test [6] to (10), the following range of gain for stability is obtained:

\[ 0 < K_e < \frac{1 + a}{1 - a} 2\pi^2 R_i C_i \]  

4 System modelling and simulation

At the design stage of the induction heating system, a simulation model of the converter and the load was developed using the SIMULINK package to estimate the turns ratio of the impedance matching transformer, the


Referring to Fig. 6 the capacitor and inverter voltages are passed through relays, which represent zero-crossing detectors (ZCD), the outputs of which are applied to the inputs of the XOR. The lowpass filter (LPF) output is compared with the reference value of 0.5 and the error is sampled by a first-order sample-and-hold, which represents the analogue-to-digital conversion operation. The discrete-time integrator implements the integral controller. The VCO output in this simulation is the square wave inverter output voltage, which is applied to the resonant load model. The rate limiter adjusts the rate of change of the inverter voltage during switches to practical values.

Fig. 7 shows sample simulation results for steady-state and transient operation of the system. In the transient test case, it is assumed that there are ramp changes in the inductance and the resistance of the coil from 90 μH to 72 μH, and from 10 Ω to 8 Ω, respectively (Section 4). This emulates a transient test on the actual system in which the workpiece is pulled out by almost 20%. In Fig. 7c it can be observed that the PLL control strategy keeps the coil current in phase with the inverter voltage under all operating conditions.

5 Experimental results

An experimental prototype of the proposed system has been set up using a Fuji IPM inverter module (7MBP 100RA-120), with short-circuit, overcurrent, overtemperature and undervoltage protection logic. The system has been operated at an output power of 19.8 kW, an operating frequency of 72 kHz and an input voltage of 500 V. The inverter output voltage and current, and the capacitor voltages of the PLL circuit (XOR and LP filter outputs) were also measured and are presented in Fig. 10. A transient test has been performed at a lower power of
3.3 kW with a different coil, where the workpiece was suddenly partially pulled out of the coil (by about 20%). The transient change in the filtered output shows that the PLL control system brings the system back to unity power factor operation in about 50 ms. It is difficult to make a comparison with the simulation result under similar conditions, since the exact conditions in the test cannot be modelled in the simulation. However, the response time in the simulation is around 30 ms, which roughly agrees with the practical result. Note that in the simulation result the transient starts at $t = 250$ ms and comes to an end at $t = 280$ ms. Comparison of steady-state experimental and

**Fig. 8** Experimental results for 19.8 kW output

a (i) Inverter voltage ($v_i$) and current ($i_i$). (ii) Inverter voltage and current, reduced timescale (1 µs/div)

b Inverter voltage ($v_i$) and capacitor voltage ($v_c$)

c Collector-emitter voltages of IGBTs on the same inverter leg
simulation results reveals that the system design based on the simulation model closely follows the predicted behaviour.

Referring to Fig. 8a, (i), it can be observed that the inverter switches at exactly zero current which ensures unity power factor. This also means that switching losses are minimised as a result of zero current switching. Hence, in efficiency calculations the switching losses can be neglected and an estimate of the overall efficiency of the inverter based on conduction losses only can be obtained, using

$$\eta = \left(1 - \frac{2V_{CE, sat}}{V_{dc}}\right) \times 100\%$$  \hspace{1cm} (12)

as 98.9%. In (12) $V_{CE, sat}$ represents the saturation voltage of the IGBTs.

Fig. 8a, (ii) displays the inverter current and voltage on a much smaller time scale and shows that the current and voltage waveforms are exactly in phase. It may also be noted that the inverter switches in 1.2 $\mu$s. Furthermore, the inverter voltage exhibits no oscillations during switching intervals. This is the result of zero-current switching and the very small leakage inductance of the impedance matching transformer. The IGBT collector–emitter voltages (for IGBTs on the same inverter leg) on a narrow time scale are shown in Fig. 8c, where it is also clear that the IGBTs switch in about 0.8 $\mu$s, which is consistent with Fig. 8b. Note that the IGBTs on the same leg switch almost simultaneously without giving rise to shoot-through, which is again a result of zero-current switching. Fig. 8b shows that the inverter and capacitor voltages are phaseshifted by 90°, which demonstrates that the PLL scheme operates successfully. The effect of increasing the dead-band duration on the inverter output voltage is illustrated in Fig. 9, where the dead-band is adjusted to 1.2 $\mu$s. The oscillations in the voltages during the switching intervals are the result of the feedback diodes trying to turn on as the load current reverses direction when the outgoing transistors are turned off. During this transition period, the incoming transistors remain off due to the increased dead-band. It is evident that such oscillations give rise to extra losses. Therefore, it can be concluded that the dead-band duration is very critical in zero-current switching applications.

6 Conclusions

A DSP-based PLL-controlled induction heating system has been described in which zero-current switching of the IGBTs and operation at unity power factor with negligible oscillations on the inverter voltage are achieved through a software-based PLL control scheme using a DSP which has a hardware dead-band feature. The proposed DSP-based
PLL controller is more flexible and precise than conventional analogue PLL controllers, allowing easy modification of control parameters (such as dead-band time and controller gain) via software, whereas in analogue implementations, which require hardware changes, these modifications would be far more difficult. The dead-band delay can be kept constant at any predefined value, independent of the operating frequency, using the built-in dead-band circuitry. Experimental results reveal that the PLL control scheme operates precisely as designed and no phase delay was observed between the inverter output voltage and current. Transient tests on the system have shown that after a disturbance the PLL control system brings the system back to unity power factor operation within a time of 50 ms.

System parameters such as the turns ratio of the impedance matching transformer, compensating capacitor value and IGBT ratings, as well as controller gain were obtained from a simulation model. Agreement between predicted simulation results and experimental results have validated the design.

The use of a DSP-based control system has the added advantage that different control schemes requiring different heating periods and different adaptations of the induction heating system can be implemented with modifications to the software alone and no changes to the hardware.

7 Acknowledgments

The authors wish to thank the Eastern Mediterranean University Technology Development Centre (DAU-TEKMER) for their financial support.

8 References


9 Appendix

The phase difference \( \phi \) can be linearized by means of the following truncated Taylor series:

\[
\phi(T) \approx \phi(T_0) + \left( \frac{d\phi}{dT} \right)_{T=T_0} (T - T_0)
\]

where \( T_0 = 2\pi/\omega_0 \). The derivative can be evaluated from (5) as

\[
\frac{d\phi}{dT} = \frac{\omega(T^2 + T_0^2)}{a(T^2 - T_0^2) + \omega^2 T^2}
\]

where \( a = 2\pi R_C \). When evaluated at \( T = T_0 \), this derivative gives

\[
\left. \frac{d\phi}{dT} \right|_{T=T_0} = -\frac{2}{\omega} a = -\frac{1}{\pi R_C}
\]

By also noting that \( \phi(T_0) = \pi/2 \), (8) is obtained.

Substituting (8) and (9) into (6) gives:

\[
\Delta x_f(k + 1) = a \Delta x_f(k) - \left( 1 - \frac{a}{\pi^2 R_C} \right) \Delta T(k)
\]

Simplification using the fact that \( b = 1 - a \) then yields

\[
\Delta x_f(k + 1) = a \Delta x_f(k) - \left( 1 - \frac{a}{\pi^2 R_C} \right) \Delta T(k)
\]

Similarly, substituting (8) and (9) into (7) gives

\[
\Delta T(k + 1) = \Delta T(k) + K_c \left[ a \left( \frac{\Delta x_f(k)}{\pi^2 R_C} \right)^2 + \left( 1 - \frac{a}{\pi^2 R_C} \right) \Delta T(k) \right]
\]

which simplifies to

\[
\Delta T(k + 1) = \left( a K_c \right) \Delta x_f(k) - \left( 1 - \frac{a}{\pi^2 R_C} \right) \Delta T(k)
\]

Equations (16) and (17) can then be written in matrix form as in (10).