

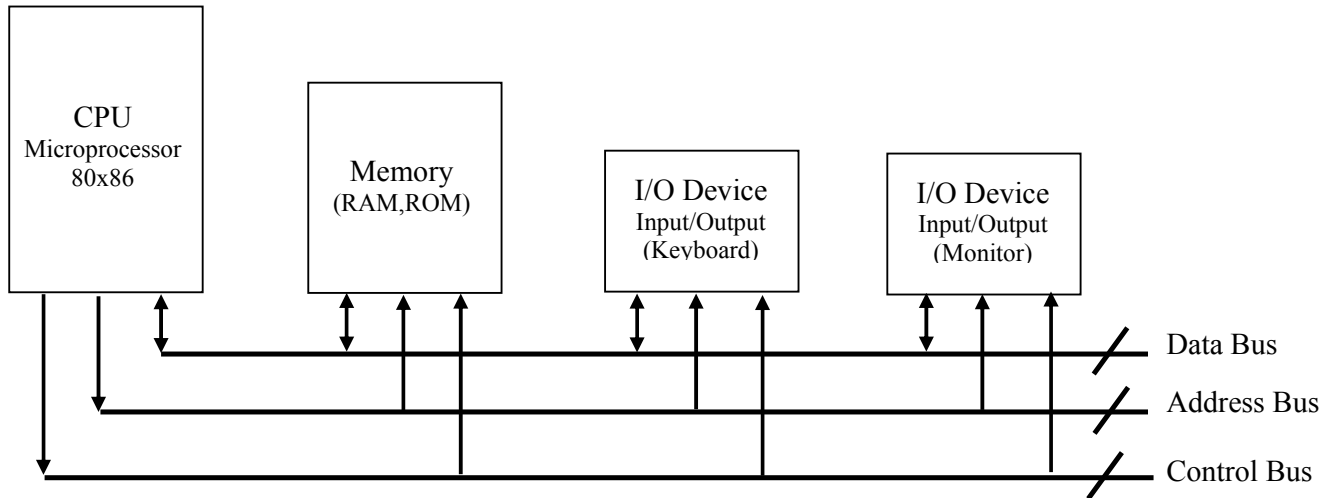
EEE 410 – Microprocessors I

Spring 04/05 – Lecture Notes # 15

Outline of the Lecture

- Basic Computer Architecture

BASIC COMPUTER ARCHITECTURE



CPU : Central Processing Unit/Microprocessor; the *Brain* and the *Heart* of the Computer. Executes (processes) the information stored in memory.

Memory : Memory is the primary storage for the programs and data (RAM, ROM)

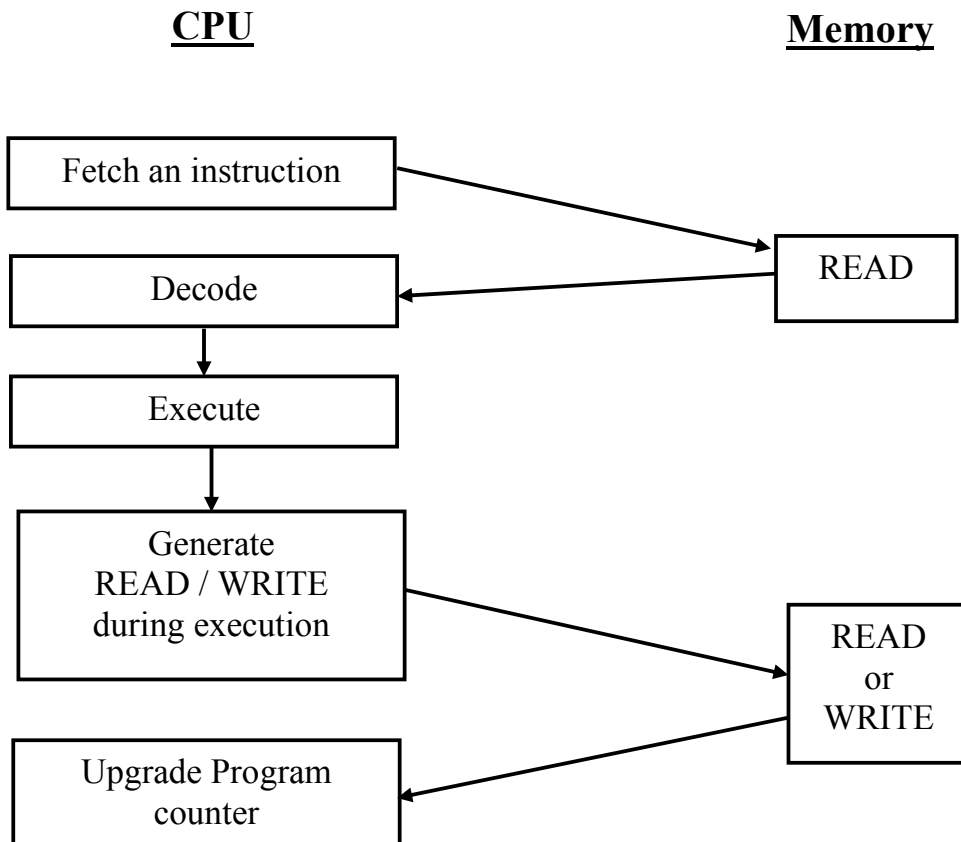
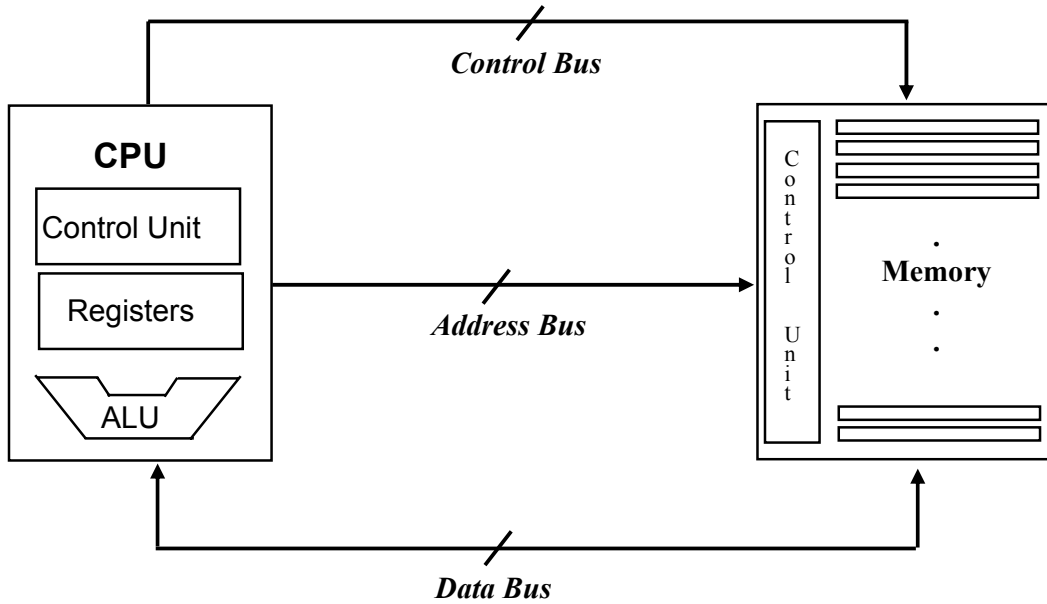
I/O :

- Drives the disks (secondary storage units): Hard Disk, Floppy Disks etc.
- Monitor (CRT –*Cathode Ray Tube*)
- Keyboard
- Printer
- Mouse
- Fax, Modem

Buses : A bus is defined to be a bundle of wires. There are 3 types of buses

- Address Bus (Unidirectional)
- Data Bus (Bidirectional)
- Control Bus (Unidirectional)

- **Time Sequencing during an instruction execution**



28	$\overline{\text{IO/M}}$ (memory or input/output)	Indicates whether the address bus is accessing memory or I/O device. In 8086, when it is high, it is accessing the memory and when it is low, it is accessing the I/O.
29	$\overline{\text{WR}}$ (Write)	Active-low output signal. Indicates that the data on the data bus is being written to memory or I/O. Used along with pin 28 for write operations.
30	HLDA (hold acknowledge)	Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that DMA (Direct Memory Access) controller can use the bus.
31	HOLD (hold)	Active-high input from the DMA controller which indicates that the device is requesting access to memory and I/O space and that the CPU should release the control of the local bus.
32	$\overline{\text{RD}}$ (Read)	Active-low output signal. Indicates that the data on the data bus is being read from the memory or I/O. Used along with pin 28 for read operations.

Basic Busses for a computer:

Every computer must have three basic busses in order to communicate: Address bus, data bus, and the control bus. The figure below shows the basic busses of 8088 based-computer. Note that the 3 control signals from 8088: $\overline{\text{WR}}$, $\overline{\text{RD}}$, and $\overline{\text{IO/M}}$ are used to generate 4 new control signals ($\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$) by using a decoder circuit.

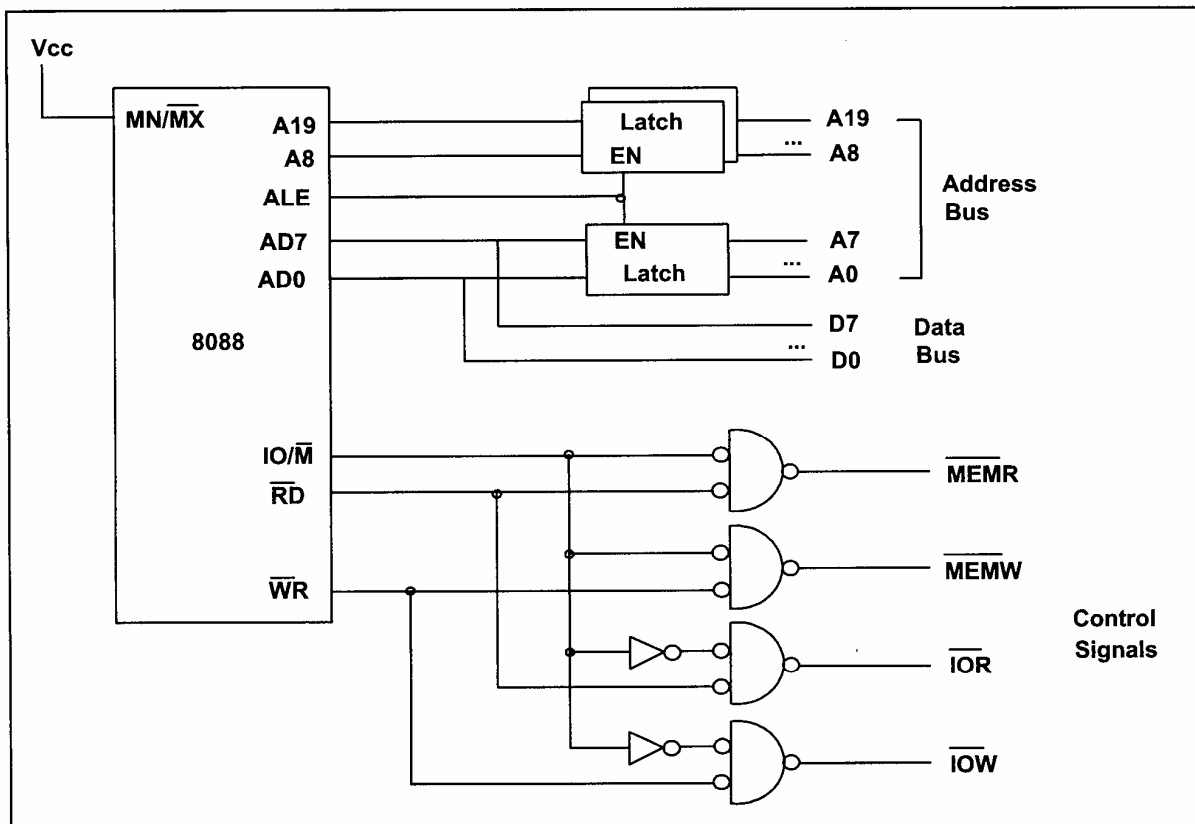


Figure 9-6. 8088 Address, Data, and Control Buses

Direct Memory Access (DMA)

In computers there is often need to transfer a large amount of data between the memory and peripherals such as hard disk. In such a case using the CPU to transfer data is too slow, since the data first must be fetched into the CPU and then sent to its destination.

For this reason Direct Memory Access controller is used to bypass the CPU and provide a direct connection between the peripherals and memory, thus transferring the data as fast as possible.